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Ulrich et al.

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(54) **BUS REVERSABLE ORTHOGONAL
DIFFERENTIAL VECTOR SIGNALING
CODES**

USPC 375/260, 288, 340; 341/81; 711/157;
712/221; 708/520; 340/870.22
See application file for complete search history.

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tional Searching Authority, mailed Nov. 5, 2012, in International
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(51) **Int. Cl.**
H04L 27/06 (2006.01)
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Primary Examiner — Rahel Guarino

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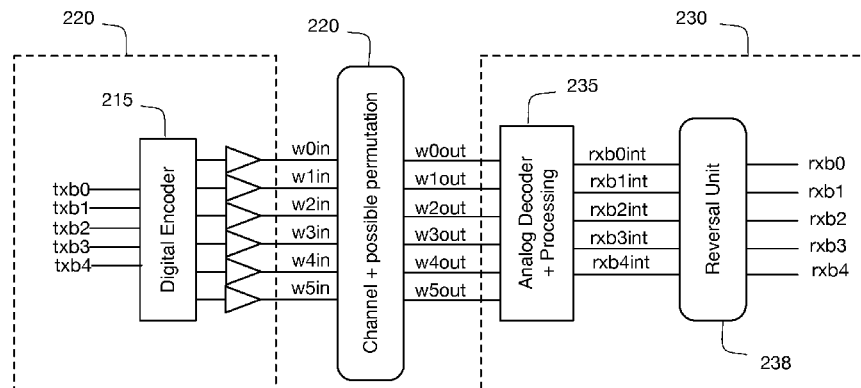
(52) **U.S. Cl.**
CPC **H04B 3/50** (2013.01)

(57) **ABSTRACT**

(58) **Field of Classification Search**
CPC . H04L 1/0057; H04L 1/0031; H04L 1/0027;
H04L 1/1893; H04L 1/0637; H04L 1/0675;
H04L 25/03898; H04L 27/3416; H04L
2025/03802; H04L 27/2601; H04L
2001/0094; H04L 1/0662; H03M 13/271;
H03M 13/2707; H03M 13/616; H03M
13/1168; H03M 13/2739; H03M 13/2753;
H04B 3/00; H04H 40/18

Properties and the construction method of Orthogonal Dif-
ferential Vector Signaling Codes are disclosed which are
tolerant of order-reversal, as may occur when physical
routing of communications channel wires causes the bus
signal order to be reversed. Operation using the described
codes with such bus-reversed signals can avoid complete
logical or physical re-ordering of received signals or other
significant duplication of receiver resources.

20 Claims, 6 Drawing Sheets



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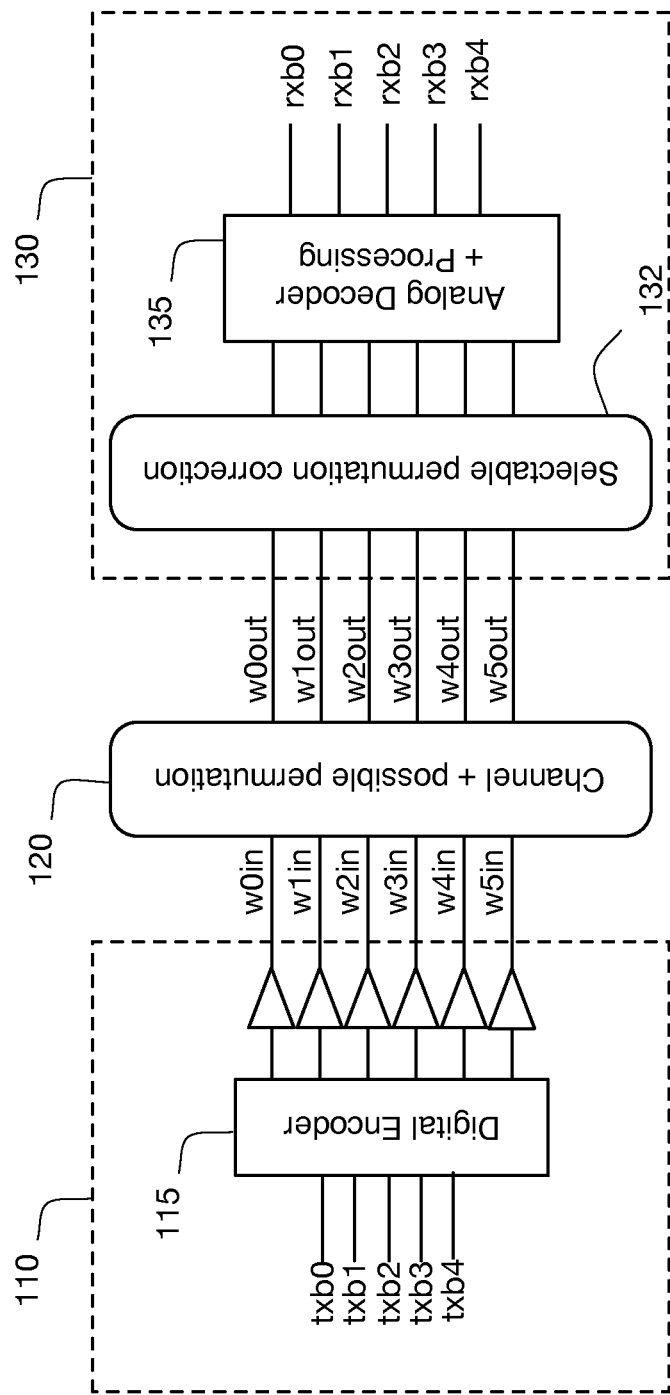


FIG. 1 (PRIOR ART)

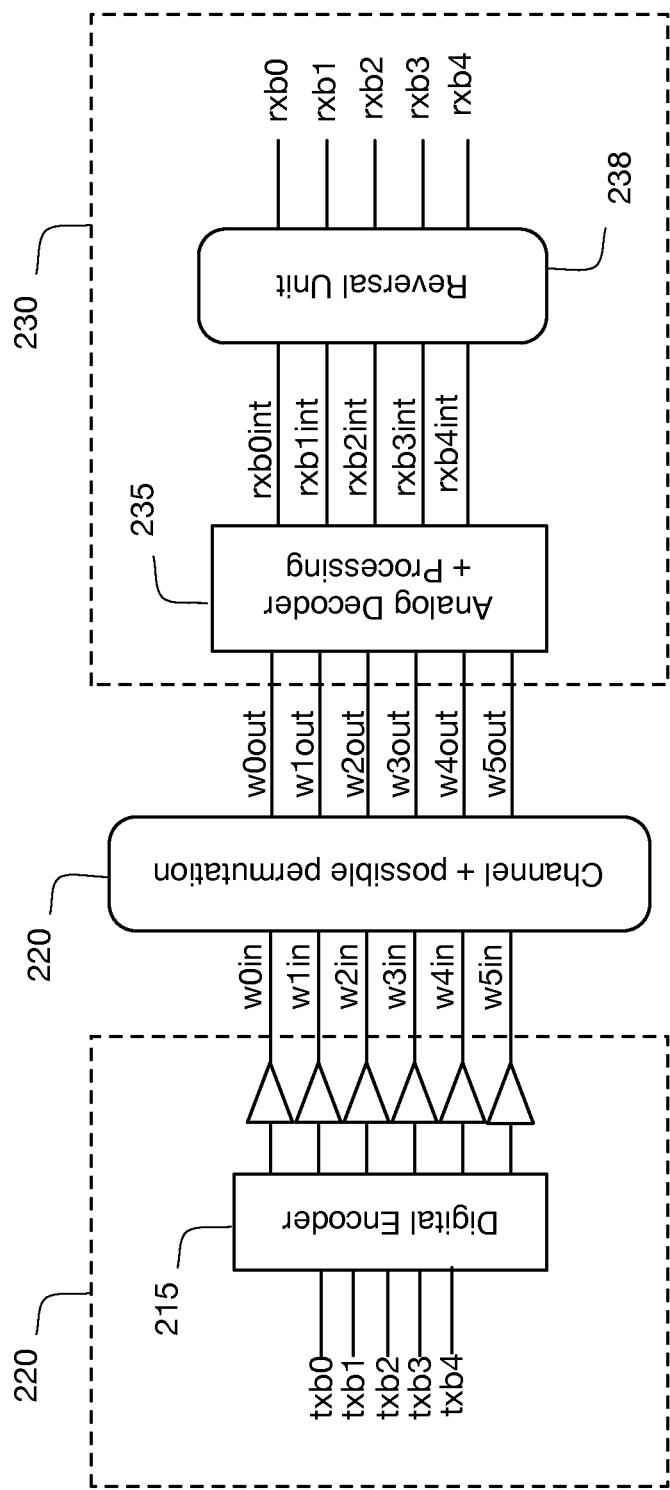


FIG. 2

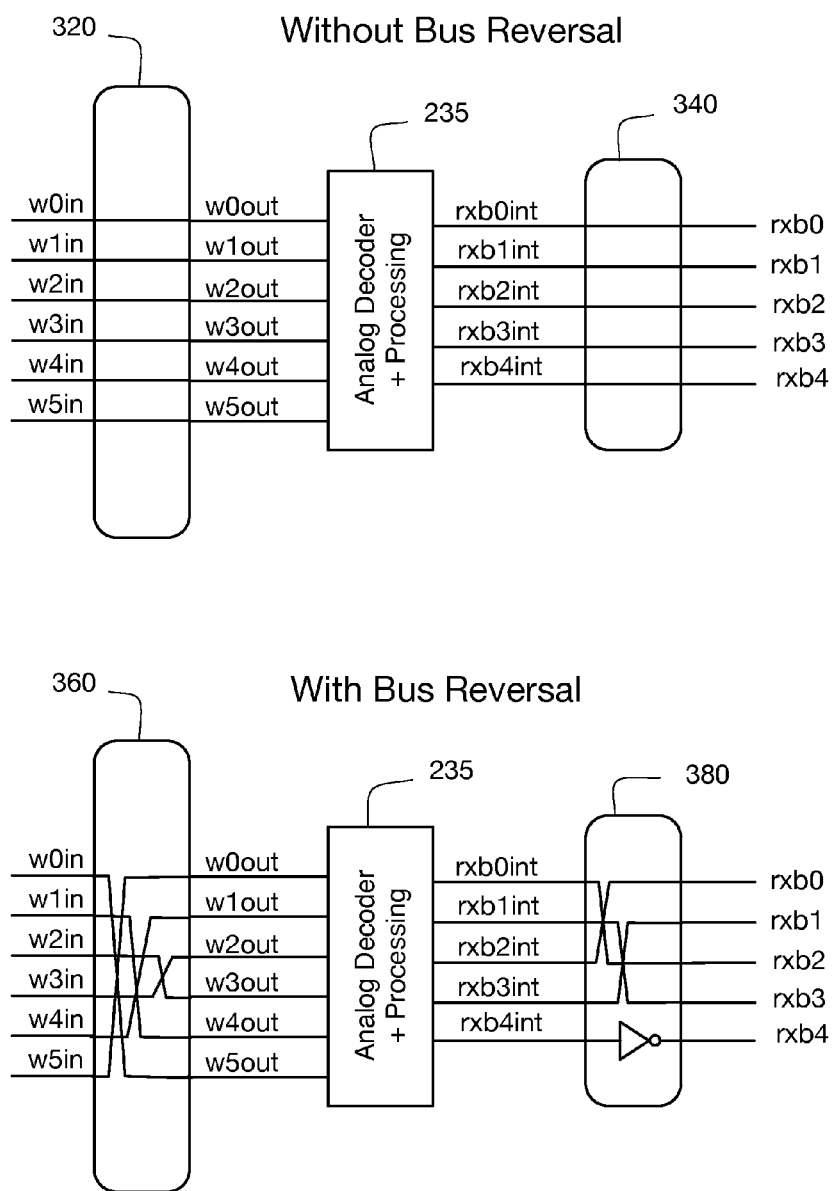


FIG. 3

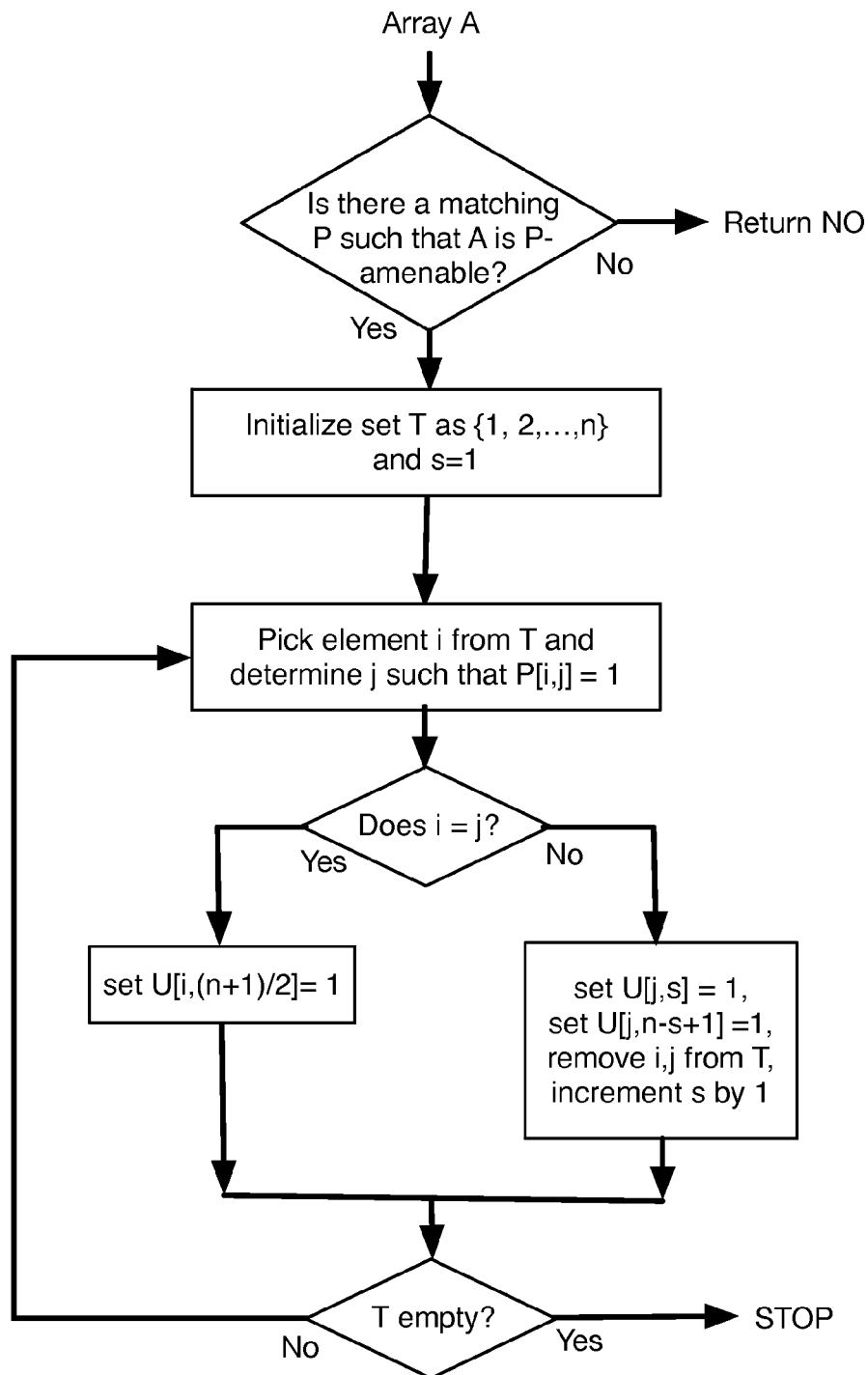


FIG. 4

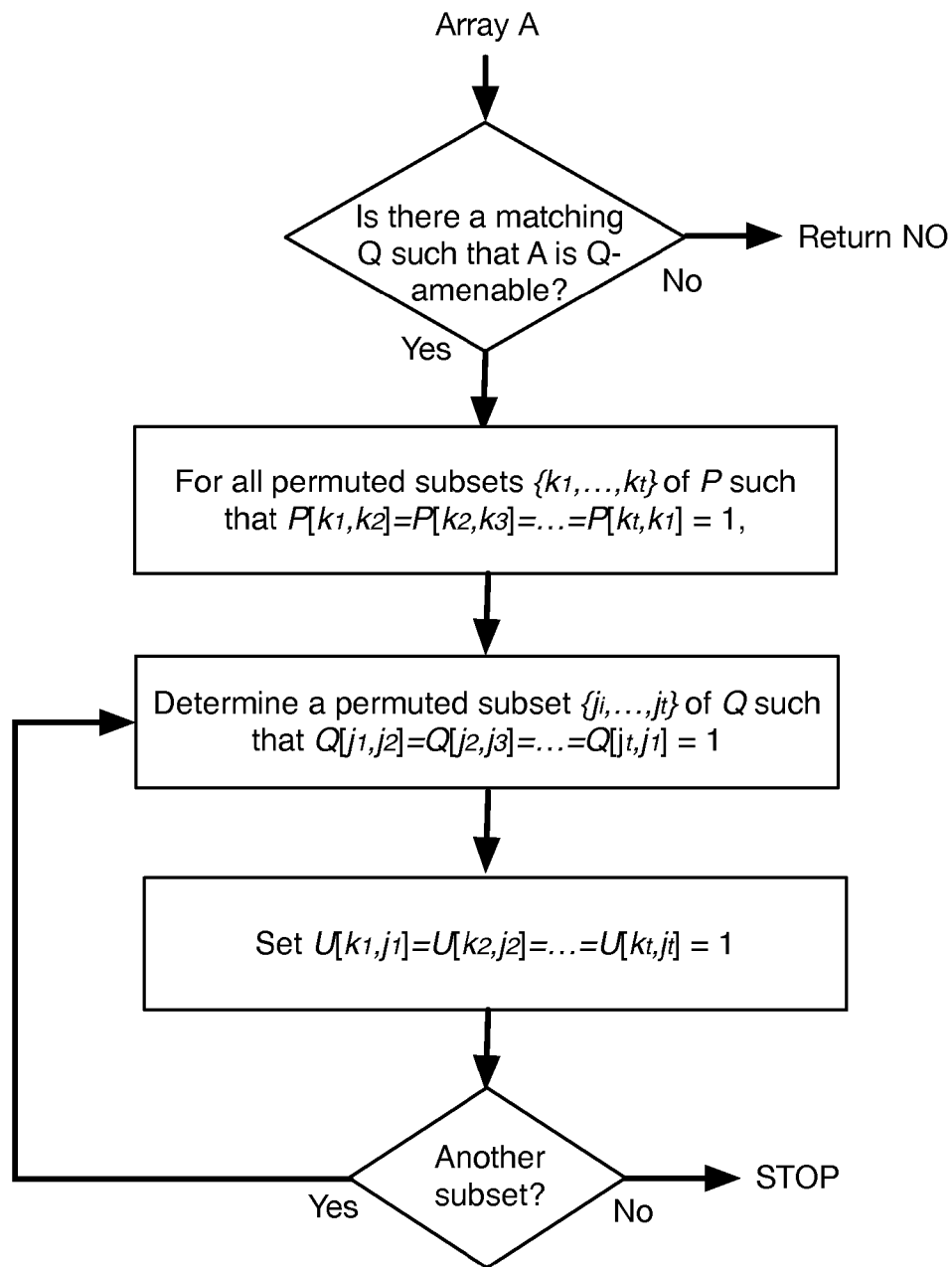


FIG. 5

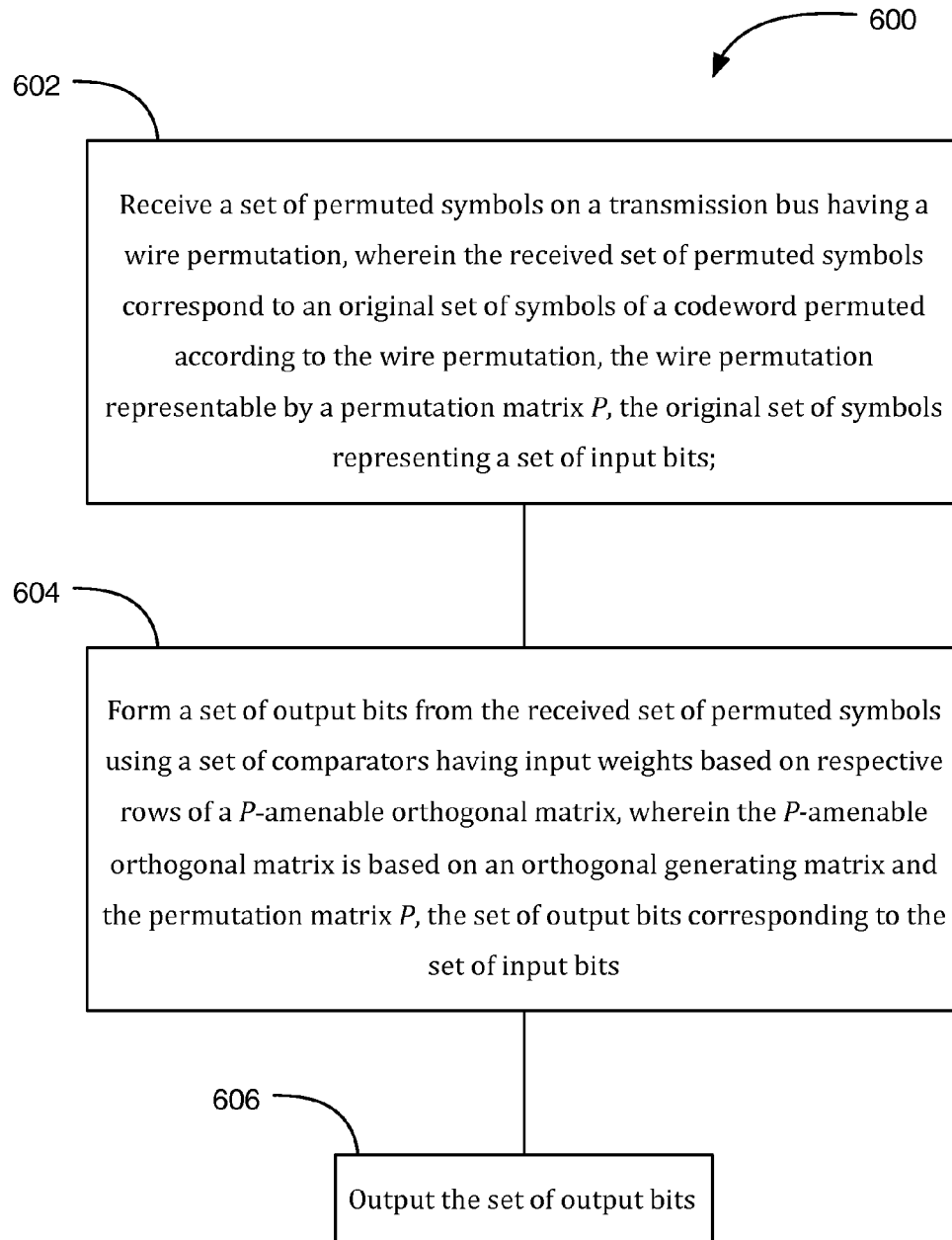


FIG. 6

BUS REVERSABLE ORTHOGONAL DIFFERENTIAL VECTOR SIGNALING CODES

This application claims priority to U.S. Provisional Patent Application 62/025,712, filed Jul. 17, 2014, naming Roger Ulrich, entitled "Bus Reversible Orthogonal Differential Vector Signaling Code" which is herein incorporated by reference in its entirety for all purposes.

REFERENCES

The following references are herein incorporated by reference in their entirety for all purposes:

U.S. Patent Publication No. 2011/0268225 of U.S. patent application Ser. No. 12/784,414, filed May 20, 2010, naming Harm Cronie and Amin Shokrollahi, entitled "Orthogonal Differential Vector Signaling" (hereinafter "Cronie I");

U.S. Patent Publication No. 2011/0302478 of U.S. patent application Ser. No. 12/982,777, filed Dec. 30, 2010, naming Harm Cronie and Amin Shokrollahi, entitled "Power and Pin Efficient Chip-to-Chip Communications with Common-Mode Rejection and SSO Resilience" (hereinafter "Cronie II");

U.S. patent application Ser. No. 13/030,027, filed Feb. 17, 2011, naming Harm Cronie, Amin Shokrollahi and Armin Tajalli, entitled "Methods and Systems for Noise Resilient, Pin-Efficient and Low Power Communications with Sparse Signaling Codes" (hereinafter "Cronie III");

U.S. Patent Publication No. 2011/0299555 of U.S. patent application Ser. No. 13/154,009, filed Jun. 6, 2011, naming Harm Cronie and Amin Shokrollahi, entitled "Error Control Coding for Orthogonal Differential Vector Signaling" (hereinafter "Cronie IV");

U.S. Provisional Patent Application No. 61/763,403, filed Feb. 11, 2013, naming John Fox, Brian Holden, Ali Hormati, Peter Hunt, John D Keay, Amin Shokrollahi, Anant Singh, Andrew Kevin John Stewart, Giuseppe Surace, and Roger Ulrich, entitled "Methods and Systems for High Bandwidth Chip-to-Chip Communications Interface" (hereinafter called "Fox I");

U.S. Provisional Patent Application No. 61/773,709, filed Mar. 6, 2013, naming John Fox, Brian Holden, Peter Hunt, John D Keay, Amin Shokrollahi, Andrew Kevin John Stewart, Giuseppe Surace, and Roger Ulrich, entitled "Methods and Systems for High Bandwidth Chip-to-Chip Communications Interface" (hereinafter called "Fox II");

U.S. Provisional Patent Application No. 61/812,667, filed Apr. 16, 2013, naming John Fox, Brian Holden, Ali Hormati, Peter Hunt, John D Keay, Amin Shokrollahi, Anant Singh, Andrew Kevin John Stewart, and Giuseppe Surace, entitled "Methods and Systems for High Bandwidth Communications Interface" (hereinafter called "Fox III");

U.S. patent application Ser. No. 13/842,740, filed Mar. 15, 2013, naming Brian Holden, Amin Shokrollahi, and Anant Singh, entitled "Methods and Systems for Skew Tolerance and Advanced Detectors for Vector Signaling Codes for Chip-to-Chip Communication" (hereinafter called "Holden I");

U.S. patent application Ser. No. 13/895,206, filed May 15, 2013, naming Roger Ulrich and Peter Hunt, entitled "Circuits for Efficient Detection of Vector Signaling Codes for Chip-to-Chip Communications using Sums of Differences" (hereinafter called "Ulrich I").

U.S. patent application Ser. No. 14/315,306, filed Jun. 25, 2014, naming Roger Ulrich, entitled "Multilevel Driver for High Speed Chip-to-Chip Communications" (hereinafter called "Ulrich II").

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U.S. Provisional Patent Application No. 61/992,711, filed May 13, 2014, naming Amin Shokrollahi, entitled "Vector Signaling Code with Improved Noise Margin" (hereinafter called "Shokrollahi I").

U.S. Provisional Patent Application No. 62/023,163, filed Jul. 10, 2014, naming Amin Shokrollahi and Roger Ulrich, entitled "Vector Signaling Code with Improved Noise Margin" (hereinafter called "Shokrollahi II").

BACKGROUND

In communication systems, a goal is to transport information from one physical location to another. It is typically desirable that the transport of this information is reliable, is fast and consumes a minimal amount of resources. One common information transfer medium is the serial communications link, which may be based on a single wire circuit relative to ground or other common reference, or multiple such circuits relative to ground or other common reference. A common example uses singled-ended signaling ("SES"). SES operates by sending a signal on one wire, and measuring the signal relative to a fixed reference at the receiver. A serial communication link may also be based on multiple circuits used in relation to each other. A common example of the latter uses differential signaling ("DS"). Differential signaling operates by sending a signal on one wire and the opposite of that signal on a matching wire. The signal information is represented by the difference between the wires, rather than their absolute values relative to ground or other fixed reference.

There are a number of signaling methods that maintain the desirable properties of DS while increasing pin efficiency over DS. Vector signaling is a method of signaling. With vector signaling, a plurality of signals on a plurality of wires is considered collectively although each of the plurality of signals might be independent. Each of the collective signals is referred to as a component and the number of plurality of wires is referred to as the "dimension" of the vector. In some embodiments, the signal on one wire is entirely dependent on the signal on another wire, as is the case with DS pairs, so in some cases the dimension of the vector might refer to the number of degrees of freedom of signals on the plurality of wires instead of exactly the number of wires in the plurality of wires.

With binary vector signaling, each component or "symbol" of the vector takes on one of two possible values. With non-binary vector signaling, each symbol has a value that is a selection from a set of more than two possible values. The set of values that a symbol of the vector may take on is called the "alphabet" of the vector signaling code. A vector signaling code, as described herein, is a collection C of vectors of the same length N, called codewords. Any suitable subset of a vector signaling code denotes a "subcode" of that code. Such a subcode may itself be a vector signaling code. Orthogonal Differential Vector Signaling codes (ODVS) as described in [Cronie I] are one specific example of a vector signaling code as used in descriptions herein.

In operation, the coordinates of the codewords are bounded, and we choose to represent them by real numbers

between -1 and 1 . The ratio between the binary logarithm of the size of C and the length N is called the pin-efficiency of the vector signaling code.

A vector signaling code is called "balanced" if for all its codewords the sum of the coordinates is always zero. Balanced vector signaling codes have several important properties. For example, as is well-known to those of skill in the art, balanced codewords lead to lower electromagnetic interference (EMI) noise than non-balanced ones. Also, if common mode resistant communication is required, it is advisable to use balanced codewords, since otherwise power is spent on generating a common mode component that is cancelled at the receiver.

Additional examples of vector signaling methods are described in Cronie I, Cronie II, Cronie III, Cronie IV, Fox I, Fox II, Fox III, Holden I, Shokrollahi I, and Hormati I.

BRIEF DESCRIPTION

Properties and the construction method of Orthogonal Differential Vector Signaling Codes are disclosed which are tolerant of order-reversal, as may occur when physical routing of communications channel wires causes the bus signal order to be reversed. Operation using the described codes with such bus-reversed signals can avoid complete logical or physical re-ordering of received signals or other significant duplication of receiver resources.

BRIEF DESCRIPTION OF FIGURES

FIG. 1 shows a prior art configuration of a transmitter and receiver interconnected by a multiwire channel that may be bus reversed.

FIG. 2 shows a system in accordance with at least one embodiment, capable of communicating information from a transmitting device to a receiving device over a communications channel which may be bus-reversed.

FIG. 3 shows one embodiment of a receiver producing received data from non-bus-reversed received signals, and producing the same received data if the received signals are bus-reversed.

FIG. 4 is a block diagram of a procedure to find reversal-amenable permutations of a matrix.

FIG. 5 is a block diagram of an additional procedure to find reversal-amenable permutations of a matrix if matrix columns are permuted.

FIG. 6 shows a method in accordance with at least one embodiment.

DETAILED DESCRIPTION

The concept of orthogonal vector signaling has been introduced in [Cronie]. As presented there, an orthogonal differential vector signaling (ODVS) code may be obtained via the multiplication

$$(0x_2, \dots, x_n) \cdot M/a \quad [\text{Eqn. 1}]$$

wherein M is an orthogonal $n \times n$ -matrix in which the sum of the columns is zero except at the first position, x_2, \dots, x_n belong to a set S describing the original modulation of these symbols, and a is a normalization constant which ensures that all the coordinates of the resulting vector are between -1 and $+1$. In the following, we call an orthogonal matrix for which the sum of the columns is zero except in the first position an "ODVS generating matrix."

For example, in case of binary modulation, the set S may be chosen to be $\{-1, +1\}$. In case of ternary modulation, the

set S may be chosen as $\{-1, 0, 1\}$, in case of quaternary modulation, the set S may be chosen as $\{-3, -1, 1, 3\}$, and in case of quintary modulation S may be chosen as $\{-2, -1, 0, 1, 2\}$.

In operation, the matrix M does not need to be orthogonal. It suffices that all its rows are pairwise orthogonal (even if the rows are not of Euclidean norm 1). In the following, we call such matrices s -orthogonal (scaled orthogonal).

For proper working of this scheme it is not necessary that all the x_i are modulated by the same set S .

Detection of the transmitted signals can be accomplished with the matrix M in the following manner. Each row of M is scaled in such a way as to ensure that the sum of the positive entries in that row is equal to 1. Then the entries of each row of the new matrix (except for the first) are used as coefficients of a multi-input comparator as defined in [Holden I]. For example, if $n=6$, the values on the 6 wires (possibly after equalization) are denoted by a, b, c, d, e, f and the row is $[1/2, 1/4, -1/2, 1/4, -1/2, 0]$, then the multi-input comparator would calculate the value

$$\frac{a}{2} + \frac{b+d}{4} - \left(\frac{c+e}{2}\right) \quad [\text{Eqn. 2}]$$

and would slice the result. In case of binary modulation, such slicing is performed by a digital comparator, whereas for higher order modulation a stack of digital comparators with distinct threshold references may be used as taught in [Shokrollahi II]. Alternatively, the result may be passed through an Analog-to-Digital converter with appropriate precision.

In a typical application using an ODVS code to communicate between two integrated circuit devices, multiple chip pins or pads are interconnected as a parallel bus. Following conventional best practice, one chip will be designed to have the required number of I/O pins sequentially assigned to the communications interface function, as one example along its rightmost package edge, and the other chip will be designed to have the same connections assigned, continuing the example, along its leftmost package edge such that a series of equal-length straight signal traces may connect the pins in consecutive order.

However, even when integrated circuit devices are designed to facilitate such optimized physical interconnection, the desired results may be impractical to achieve in practice. The physical placement of the two chips may preclude direct equal-length connections, requiring trace routing at right angles or using vias, which introduce impedance anomalies and signal path length differences. In the worst case, often occurring with "flip chip" packaging and/or active-both-sides PCB designs, the only available routing path between the two devices results in the sequential order of the I/O pin signals being reversed between the two devices. Such situations may also occur if symmetrical "plug in either way" connectors are used for interconnections. This is typically referred to as "bus reversal" since effectively the signals on the wires are presented to the receiver in reversed sequential order.

FIG. 1 illustrates a prior art transmitting device 110 connected to a receiving device 130 via a multiwire channel 120 which may (or may not) be bus reversed. If the bus is not reversed, transmitted channel signals $w0_{in}, \dots, w5_{in}$ correspond directly to received channel signals $w0_{out}, \dots, w5_{out}$. If the bus is reversed, the signal $w0_{in}$ appears at $w5_{out}$, $w1_{in}$ appears at $w4_{out}$, $w2_{in}$ appears at

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w3out, w3in appears at w2out, w4in appears at w1out, and w5in appears at w0out. To insure that received data rxb0-rxb4 in receiving device 130 duplicates transmitted data txb0-txb4 in the transmitting device, receiver 130 must include a selectable permutation device 132 to permute the received signal order back to its intended order, prior to analog detection and processing 135.

Such known solutions for bus reversal generally rely on physical reordering of the received bus signals using analog multiplexers or other steering logic at the input of the receiving chip, at the cost of significant receiver complexity. At very high signaling rates, these additional circuit elements introduce impedance anomalies leading to signal degradation. Moreover, it may be impractical to route the necessary signals from one end of the bus across the receiver chip to multiplexers at the other end of the bus to perform such physical bus reordering and still meet timing constraints. Similarly, even though the receiver is typically aware of a reversed bus, it may not be practical to include both a receiver for when the bus wires are reversed, and one for the case of normal operation, as this will lead to area and power penalties.

One familiar with the art may observe that some known art receive solutions, such as use of single-ended line receivers to detect incoming signals, might permit the selectable permutation device 132 to operate in the digital domain, after the line receivers. However, such solutions will not in general be available if differential receivers are used, as will often be the case for high speed, high performance interconnections.

Furthermore, if an ODVS code is used, ignoring bus reversal may have a disastrous effect on differentially detected received signals. For example, consider an ODVS code generated by the s-orthogonal matrix M given below:

$$M = \begin{pmatrix} 1 & 1 & 1 \\ 1 & -1 & 0 \\ 1 & 1 & -2 \end{pmatrix}. \quad [\text{Eqn. 3}]$$

Consider the encoding of the vector (0, 1, -1) as the codeword (0, 1, -1) (after normalization by division by 2, i.e., with a=2 in Eqn. 1). A bus-reversed communications channel would transform this vector into (-1, 1, 0), which is not even a valid codeword. Trying to detect this codeword with the comparators (1,-1,0) and (1/2, 1/2, -1) would lead to the vector (0, -2, 0) which is not the same as the original encoded vector (and cannot even be detected reliably because the last "0" in the vector introduces an ambiguous comparator state.)

However, ODVS code embodiments also exist where bus reversal does not have a disastrous effect and for which compensation can be very efficiently applied using simple digital logic. In one such embodiment, the ODVS code is generated by the Hadamard matrix

$$H = \begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 1 & -1 \\ 1 & 1 & -1 & -1 \\ 1 & -1 & -1 & 1 \end{pmatrix}. \quad [\text{Eqn. 4}]$$

A vector (0,x, y, z) is encoded with this matrix to

$$((x+y+z)/a, (y-x-z)/a, (x-y-z)/3, (z-x-y)/a) \quad [\text{Eqn. 5}]$$

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wherein a is chosen to normalize the resulting values to the range -1 to +1. Bus reversal transforms these values into a set of permuted symbols corresponding to

$$((z-x-y)/a, (x-y-z)/a, (y-x-z)/a, (x+y+z)/a) \quad [\text{Eqn. 5}]$$

and final detection of this vector by the comparators (1, -1, 1, -1)/2, (1,1,-1,-1)/2, and (1,-1,-1,1)/2 yields the vector

$$2(-x, -y, z)/a. \quad [\text{Eqn. 6}]$$

This is, up to a sign change on the first two entries and scaling, equal to the original bits (x, y, z). This sign change can be easily implemented in digital logic after detection of the signals by the analog receiver. A sign change may correspond to a binary inversion, a signal negation, or any other relevant sign changes known to one of skill in the art.

We call an ODVS code "reversal-amenable" if bus reversal has a similar effect on the signals as for the matrix H. This means that a wire permutation (including but not limited to a full bus reversal) of a codeword, followed by the comparators given by the matrix produces a possibly permuted vector of input bits in which some of the entries may have a reversed sign. An orthogonal generating matrix that generates such an ODVS code is called "reversal-amenable." In applications, a reversal-amenable ODVS code may be preferable to one that is not reversal-amenable. Even if some permutation of the resulting received bits is required to return to non-bus-reversed order, the amount of permutation required will be less than the full bus reversal required by prior art solutions, such permutation may be performed by post-detection digital logic (versus by analog circuitry at the chip input) and, for embodiments using multiple phases of receive signal processing, the required permutations and sign reversals can be done at lower speed within each of the multiple processing phases. Embodiments requiring an explicit decoding operation to recover received data from the detected signals may also advantageously incorporate the required permutation and negation operations for compensation for bus reversal into the decoder logic.

A system incorporating such a reversal-amenable ODVS code in accordance with at least one embodiment is illustrated in FIG. 2. Transmitting device 220 encodes transmit data txb0, . . . , txb4 to produce an ODVS code, which is emitted as signals w0in, . . . , w5in to communications channel 220. Communications channel 220 may or may not reverse the consecutive ordering of signals w0in, . . . , w5in during transmission to w0out, . . . , w5out, where they are received by receiving device 230. Without explicit permutation or other controllable redirection being performed on the received signals, analog decoder and processing devices shown as 235, which may include without limitation differential line receivers, comparators, multi-input comparators and other analog processing elements detects received signals rxb0int, . . . , rxb4int, which are subsequently processed by digital reversing unit 238 to obtain the received signals rxb0, . . . , rxb4.

Construction of Reversal-Amenable ODVS Codes

In some cases, a reversal-amenable ODVS code may be obtained from a general ODVS code by judiciously permuting the columns of the generating matrix Min Eqn. 1. For example, by permuting columns 2 and 3 of the matrix M in Eqn. 3, we obtain a reversal-amenable ODVS code: A vector (0,x, y) is encoded with the new matrix to a set of original symbols (x+y, -2y, y-x)/a, wherein a is chosen to make sure that the entries of this vector are between -1 and +1. Application of bus reversal leads to the vector of permuted symbols (y-x, -2y, x+y)/a, and final detection via the

comparators (1,0,-1), (1/2,-1, 1/2) leads to the vector of output bits $(-2x, 3y)/a$ which is (up to scaling and sign) equal to the original bits.

The following description is of a method to detect whether an orthogonal generating matrix generating an ODVS code can be made reversal-amenable by a permutation of the columns, and for finding a right permutation of the columns that allows this. To this end, the descriptive terminology of matrices and permutations is used herein, as described in standard textbooks on linear algebra and group theory.

A quadratic matrix is called "monomial" if it has exactly one nonzero entry in every row and every column. It is called a "permutation matrix" if it is monomial and the nonzero entry in every row and column is 1. If A is any matrix with n columns and P is a permutation matrix with n rows, then A·P is obtained by permuting the columns of A according to P. Similarly, if A has n rows, then P·A is obtained from A by permuting the rows of A according to P.

The "reversal" matrix R with n rows and columns is the matrix

$$R = \begin{pmatrix} 0 & 0 & \dots & 0 & 1 \\ 0 & 0 & \dots & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 1 & \dots & 0 & 0 \\ 1 & 0 & \dots & 0 & 0 \end{pmatrix} \quad [\text{Eqn. 7}]$$

i.e., the matrix has only 1's on its main anti-diagonal and is zero elsewhere.

An ODVS generating matrix A is called "P-amenable" if $A \cdot P \cdot A^T$ is a monomial matrix, wherein A^T is the transpose of A and P is a permutation matrix. If A is P-amenable, then a wire permutation corresponding to a permutation of the communication wires according to the matrix P can be easily adjusted at the receiver: the codewords of the ODVS code generated by A are the vectors $(0|x) \cdot A/a$, wherein x is a vector of length n-1 (if A has size n) and a is a normalization constant. Permutation of this result by P, and detection of the results corresponds to the multiplication of the new result by $A^T \cdot D$, where D is the diagonal matrix that has as its k-th diagonal entry the sum of the positive entries of the k-th row of A. In total, therefore, the coding and detection of the signals in the presence of a permutation of the wires according to P corresponds to the multiplication

$$(0|x) \cdot A \cdot P \cdot A^T \cdot D/a. \quad [\text{Eqn. 8}]$$

The input vector x can now be re-assembled if $A \cdot P \cdot A^T$ is a monomial matrix.

As can be seen by anyone of moderate skill in the art, a reversal-amenable ODVS code is one that is generated by an R-amenable matrix A.

A procedure is now described to compute a permutation matrix U (if it exists) such that A·U is R-amenable. Constructing the ODVS code using A·U would then lead to a reversal-amenable ODVS code. To this end, we call a permutation matrix P with n rows a "matching" if P² is the identity matrix and either there is no j such that P[j,j]=1 (in case n is even) or there is exactly one j such that P[j,j]=1 (in case n is odd). Here and in the following A[i,j] denotes the (i,j)-entry of matrix A. As is known to those who are somewhat versed in the theory of finite groups, or even only

the theory of permutation groups, a matrix P is a matching if and only if there is a permutation matrix U such that $U \cdot P \cdot U^T = R$.

Step 1: Determine whether there is a matching P such that A is P-amenable (for example by calculating $A \cdot P \cdot A^T$ for all matchings P via the procedure below and checking whether the result is monomial).

Step 2: If there is no such matching P, return NO.

Step 3: If there is such a matching P, then proceed as follows:

Step 3.1: Initialize set T as $\{1, 2, \dots, n\}$ and s=1.

Step 3.2: Pick an element i from T and determine j such that P[i,j]=1.

Step 3.2.1: if j=i, then (necessarily n is odd) set $U[j, (n+1)/2] = 1$.

Step 3.2.2: if j≠i, then set $U[i,s]=1$, $U[j, n-s+1]=1$, remove i,j from T, and increase s by 1.

Step 3.2.3: If T is empty, stop, else go to Step 3.2.

This procedure is illustrated as the block diagram of FIG.

4. Amenability to Arbitrary Permutations

In the discussions above we concentrated mostly on reversal-amenable ODVS codes. However, the techniques described can be used to check whether there is a permutation of the columns of an ODVS generating matrix to make it amenable to a given wire permutation, and if so, to calculate one such permutation.

As is known to those of moderate skill in the art, any permutation matrix can be written as a product of disjoint "cycles" wherein a cycle is a permutation matrix cyclically permuting the elements of a subset of $\{1, \dots, n\}$ (called "permuted subset") and leaving all other elements of this set invariant. The size of the permuted subset is called the "length" of the cycles. Such cycles are called disjoint if the permuted subsets of the cycles are all disjoint. The "cycle structure" of a permutation matrix is the vector obtained from the lengths of the disjoint cycles the product of which is the given permutation matrix.

As is taught by the theory of finite permutation groups, for two permutation matrices P and P' there is a permutation matrix U such that $P' = U \cdot P \cdot U^T$ if and only if P and P' have the same cycle structure.

The procedure above to check whether an ODVS matrix is reversal-amenable can therefore be modified by those of skill in the art to check whether there is a permutation of the columns that makes an ODVS matrix amenable to any permutation matrix P, and to compute the permutation. One example of such an additional procedure is:

Step 1: Determine whether there is a matching Q with the same cycle structure as P such that A is Q-amenable (for example by calculating $A \cdot Q \cdot A^T$ for all permutations Q that have the same cycle structure as P and checking whether the result is monomial).

Step 2: If there is no such matching Q, return NO.

Step 3: If there is such a matching Q, then proceed as follows:

Step 3.1: For all permuted subsets $\{k_1, \dots, k_r\}$ of P such that $P[k_1, k_2] = P[k_2, k_3] = \dots = P[k_r, k_1] = 1$,

Step 3.1.1: determine a permuted subset $\{j_1, \dots, j_r\}$ of Q such that $Q[j_1, j_2] = Q[j_2, j_3] = \dots = Q[j_r, j_1] = 1$,

Step 3.1.2: set $U[k_1, j_1] = U[k_2, j_2] = \dots = U[k_r, j_r] = 1$, next subset.

This additional procedure is illustrated as the block diagram of FIG. 5.

Examples for Reversal-amenable

For the following examples we will use the following economical representation of permutation matrices via vec-

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tors. Specifically, a vector $[a_1, a_2, \dots, a_n]$ with a_1, a_2, \dots, a_n in $\{1, 2, \dots, n\}$ corresponds to the matrix having ones in positions $(1, a_1), (2, a_2), \dots, (n, a_n)$. So, for example, the vector $[2, 3, 1]$ would correspond to the permutation matrix

$$\begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{pmatrix} \quad [\text{Eqn. 9}]$$

A first example embodiment is an ODVS code generated by the matrix previously described in [Shokrollahi II]:

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & -2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 1 & 1 & -2 \\ 1 & 1 & 1 & 1 & -1 & -1 \end{pmatrix} \quad [\text{Eqn. 10}]$$

In this case there is no matching P such that $M \cdot P \cdot M^T$ is diagonal but there are exactly two matching P for which this matrix is monomial. Of these two, one, namely $P=[4,5,6,1,2,3]$ has the property that $M \cdot P \cdot M^T$ has only one negative entry (corresponding to negating a bit in case of a bus reversal):

$$M \cdot P \cdot M^T = \begin{pmatrix} 6 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 6 & 0 \\ 0 & 2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 6 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -6 \end{pmatrix} \quad [\text{Eqn. 11}]$$

Applying the procedure above leads to a matrix U and new ODVS code generating matrix M·U which is the result of permuting columns 4 and 6 of the matrix M:

$$M \cdot U = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 1 & 1 & -2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & -2 & 1 & 1 \\ 1 & 1 & 1 & -1 & -1 & 1 \end{pmatrix} \quad [\text{Eqn. 12}]$$

As illustrated in FIG. 3, the ODVS code generated by M·U, allows a receiving device (such as previously shown as 230 in the system diagram of FIG. 2) to tolerate bus reversal. Without bus reversal, communications channel 320 delivers transmitted signals $w0_{in}, \dots, w5_{in}$ directly and without permutation to $w0_{out}, \dots, w5_{out}$, allowing the analog decoder and processing of 235 to detect received signals $rxb0_{int}, \dots, rxb4_{int}$, which are passed directly through reversal unit 340 to received data $rxb0, \dots, rxb5$. When bus reversal occurs, communications channel 360 reverses the ordering of transmitted signals $w0_{in}, \dots, w5_{in}$ to $w0_{out}, \dots, w5_{out}$. However, the structure of the reversal-tolerant ODVS code permits analog decoder and processing

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235 to detect valid information despite the bus reversed received data. In this example, the proper received data $rxb0, \dots, rxb4$ is obtained if reversal unit 380 exchanges bits 1 and 3, exchanges bits 2 and 4, and negates bit 5. In at least one embodiment, negating comprises binary inversion, i.e. flipping a '0' to a '1', or a '1' to a '0'. In another embodiment, negating comprises flipping the sign of a value, i.e. a '+1' to a '-1', or a '-1' to a '+1'. However, embodiments should not be so limited.

10 In other words, if the input bits are (x_1, \dots, x_5) , then the output of the receiver is $(x_3, x_4, x_1, x_2, -x_5)$. The codewords of this code (herein subsequently called the "Glasswing code") are given in Table 1.

TABLE 1

15	$\pm[1, 1/3, -1/3, -1, -1/3, 1/3]$	$\pm[1, 1/3, -1/3, 1/3, -1, -1/3]$
	$\pm[1/3, 1, -1/3, -1, -1/3, 1/3]$	$\pm[1/3, 1, -1/3, 1/3, -1, -1/3]$
	$\pm[1/3, -1/3, 1, -1, -1/3, 1/3]$	$\pm[1/3, -1/3, 1, 1/3, -1, -1/3]$
	$\pm[-1/3, 1/3, 1, -1, -1/3, 1/3]$	$\pm[-1/3, 1/3, 1, 1/3, -1, -1/3]$
20	$\pm[1, 1/3, -1/3, -1, 1/3, -1/3]$	$\pm[1, 1/3, -1/3, 1/3, -1/3, -1]$
	$\pm[1/3, 1, -1/3, -1, 1/3, -1/3]$	$\pm[1/3, 1, -1/3, 1/3, -1/3, -1]$
	$\pm[1/3, -1/3, 1, -1, 1/3, -1/3]$	$\pm[1/3, -1/3, 1, 1/3, -1/3, -1]$
	$\pm[-1/3, 1/3, 1, -1, 1/3, -1/3]$	$\pm[-1/3, 1/3, 1, 1/3, -1/3, -1]$

25 One embodiment of an encoder for this code accepts 5 input bits a, b, c, d, e and produces 6 pairs of bits $[x_1, y_1], \dots, [x_6, y_6]$. The operational meaning of these bit pairs is that a pair $[x, y]$ corresponds to the value $-(2 \cdot (-1)^x + (-1)^y)/3$ on the corresponding wire. The encoding is then given as follows:

$$[x_1, y_1] = [\text{mux}(\text{NOR}(a, b), \text{NAND}(a, b), e), a \oplus b \oplus \neg e] \quad [\text{Eqn. 13}]$$

$$[x_2, y_2] = [\text{mux}(\text{NOR}(\neg a, b), \text{NAND}(\neg a, b), e), a \oplus b \oplus e] \quad [\text{Eqn. 14}]$$

$$35 [x_3, y_3] = [b, \neg e] \quad [\text{Eqn. 15}]$$

$$[x_4, y_4] = [d, e] \quad [\text{Eqn. 16}]$$

$$40 [x_5, y_5] = [\text{mux}(\text{NOR}(\neg c, d), \text{NAND}(\neg c, d), \neg e), c \oplus d \oplus \neg e] \quad [\text{Eqn. 17}]$$

$$[x_6, y_6] = [\text{mux}(\text{NOR}(c, d), \text{NAND}(c, d), \neg e), c \oplus d \oplus e] \quad [\text{Eqn. 18}]$$

Here, $\text{mux}(x, y, e)$ is x if $e=1$ and it is y if $e=0$. Moreover, $\neg a$ is the inverse of a and \neg is the XOR operation.

45 A second embodiment is a code for 3 wires, derived from the matrix M_1 from Eqn. 3. Applying the procedure above, the matrix

$$50 M' = \begin{pmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -2 & 1 \end{pmatrix} \quad [\text{Eqn. 19}]$$

is produced, which may be seen to be reversal-amenable. If x_1, x_2 denote the input bits, then the output of the receiver in the presence of a bus reversal is $-x_1, x_2$.

One example of a non reversal-amenable code for 4 wires may be seen by considering the generating matrix M of Eqn. 20

$$65 M = \begin{pmatrix} 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 \\ 1 & 1 & -2 & 0 \\ 1 & 1 & 1 & -3 \end{pmatrix} \quad [\text{Eqn. 20}]$$

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In this case, there is no matching P for which $M \cdot P \cdot M^T$ is monomial. This matrix and the corresponding OPDVS code is therefore not reversal-amenable.

A third example embodiment is an ODVS code for five wires generated by the matrix

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -4 \end{pmatrix} \quad [\text{Eqn. 21}]$$

as previously described in [Shokrollahi II]. Applying the procedure above, the matrix M' given as

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & -1 & 0 & -1 & 1 \\ 1 & 1 & -4 & 1 & 1 \end{pmatrix} \quad [\text{Eqn. 22}]$$

has the property that the associated ODVS code is reversal-amenable. If x_1, \dots, x_4 denote the input bits, then the output bits of the receiver in the presence of a wire permutation corresponding to a bus reversal is $-x_1, -x_2, x_3, x_4$ thus requiring only two signal negations (as one example, using two XOR gates to perform the necessary negations,) to recover the original data during bus-reversed operation.

A fourth example embodiment is of an ODVS code for 6 wires generated by the matrix previously described in [Shokrollahi II]

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1 & 1 & -1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 1 & -2 & -2 \end{pmatrix} \quad [\text{Eqn. 23}]$$

Applying the procedure above, the matrix M' given as

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 1 & -1 & 0 & 0 & -1 & 1 \\ 1 & 1 & -2 & -2 & 1 & 1 \end{pmatrix} \quad [\text{Eqn. 24}]$$

has the property that the associated ODVS code is reversal-amenable. In case of a wire permutation corresponding to a bus reversal, the first three bits need to be inverted. In other words, if x_1, \dots, x_5 denote the input bits, then the output of the receiver in the presence of a bus reversal is $-x_1, -x_2, -x_3, x_4, x_5$.

A fifth example embodiment is of an ODVS code for 9 wires generated by the matrix previously described in [Shokrollahi II]:

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$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -1 & -1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -8 \end{pmatrix} \quad [\text{Eqn. 25}]$$

Applying the procedure above, the matrix M' given as

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 1 & -1 & 0 & -1 & 1 & 0 & 0 \\ 1 & 1 & -1 & -1 & 0 & -1 & -1 & 1 & 1 \\ 1 & 1 & 1 & 1 & -8 & 1 & 1 & 1 & 1 \end{pmatrix} \quad [\text{Eqn. 26}]$$

is reversal-amenable. If x_1, \dots, x_8 denote the input bits, then the output of the receiver in the presence of a bus reversal is $-x_1, -x_2, -x_3, -x_4, x_5, x_6, x_7, x_8$.

There are several interesting matching P such that $M \cdot P \cdot M^T$ is monomial. For example, using $P=[5, 6, 7, 8, 1, 2, 3, 4, 9]$ yields a new matrix M'

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -1 & 1 \\ 0 & 0 & 0 & 0 & 0 & -1 & 1 & 0 & 0 \\ 1 & 1 & -1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -1 & -1 & 1 & 1 \\ 1 & 1 & 1 & 1 & 0 & -1 & -1 & -1 & -1 \\ 1 & 1 & 1 & 1 & -8 & 1 & 1 & 1 & 1 \end{pmatrix} \quad [\text{Eqn. 27}]$$

which is also reversal-amenable. In this case, the output of the receiver in the presence of a bus reversal is $x_3, x_4, x_1, x_2, x_6, x_5, -x_7, x_8$ so only one negation is necessary to obtain the original bits, at the cost of some additional data reordering.

The examples presented herein illustrate the use of orthogonal differential vector signaling codes for point-to-point interconnection of a transmitting device and a receiving device for descriptive simplicity. However, this should not be seen in any way as limiting the scope of any described embodiments. The methods disclosed in this application are equally applicable to other interconnection topologies, including multi-drop and star-wired interconnection of more than two devices, and other communications protocols including full-duplex as well as half-duplex and simplex communications. Similarly, wired communications are used as illustrative examples, with other embodiments also being applicable to other communication media including optical, capacitive, inductive, and wireless communications. Thus, descriptive terms such as "voltage" or "signal level" should be considered to include equivalents in other

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measurement systems, such as “optical intensity”, “RF modulation”, etc. As used herein, the term “physical signal” includes any suitable behavior and/or attribute of a physical phenomenon capable of conveying information. Physical signals may be tangible and non-transitory.

Embodiments

As shown in FIG. 6, a method 600 in accordance with at least one embodiment, comprises receiving, in step 602, a set of permuted symbols on a transmission bus having a wire permutation, wherein the received set of permuted symbols correspond to an original set of symbols of a codeword permuted according to the wire permutation, the wire permutation representable by a permutation matrix P, the original set of symbols representing a set of input bits, forming, in step 604, a set of output bits from the received set of permuted symbols using a set of comparators having input weights based on respective rows of a P-amenable orthogonal matrix, wherein the P-amenable orthogonal matrix is based on an orthogonal generating matrix and the permutation matrix P, the set of output bits corresponding to the set of input bits, and outputting, in step 606, the set of output bits.

In at least one embodiment forming the set of output bits further comprises generating a set of comparator outputs, wherein the comparator outputs correspond to the output bits.

In at least one embodiment, forming the set of output bits further comprises generating a set of comparator outputs, and performing a logical reordering of the set of comparator outputs.

In at least one embodiment, forming the set of output bits further comprises generating a set of comparator outputs, and performing a binary inversion of at least one of the comparator outputs.

In at least one embodiment, the codeword is part of an Orthogonal Differential Vector Signaling (ODVS) code.

In at least one embodiment, the P-amenable orthogonal matrix is representable as:

$$M' = \begin{pmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -2 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2]$, a set of comparator outputs represented as $[-x_1 \ x_2]$, forming the set of output bits comprises a binary inversion of comparator output $-x_1$.

In another embodiment, the P-amenable orthogonal matrix is representable as:

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & -1 & 0 & -1 & 1 \\ 1 & 1 & -4 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4]$ a set of comparator outputs represented as $[-x_1 \ -x_2 \ x_3 \ x_4]$, forming the set of output bits comprises a binary inversion of comparator outputs $-x_1$ and $-x_2$.

In another embodiment, the P-amenable orthogonal matrix is representable as:

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$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 1 & -1 & 0 & 0 & -1 & 1 \\ 1 & 1 & -2 & -2 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4 \ x_5]$, a set of comparator outputs represented as $[-x_1 \ -x_2 \ -x_3 \ x_4 \ x_5]$, forming the set of output bits comprises a binary inversion of comparator outputs $-x_1$, $-x_2$, and $-x_3$.

In at least one embodiment, the permutation matrix P is represented as:

$$P = \begin{pmatrix} 0 & 0 & \dots & 0 & 1 \\ 0 & 0 & \dots & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 1 & \dots & 0 & 0 \\ 1 & 0 & \dots & 0 & 0 \end{pmatrix},$$

corresponding to a full transmission bus reversal.

In at least one embodiment, the permutation matrix P is represented as:

$$P = \begin{pmatrix} 1 & 0 & \dots & 0 & 0 \\ 0 & 1 & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & \dots & 0 & 1 \end{pmatrix},$$

corresponding to no transmission bus permutation.

In accordance with at least one embodiment, an apparatus comprises a transmission bus configured to receive a set of permuted symbols, wherein the permuted symbols represent a wire permutation of a set of original symbols based on a permutation matrix P, the wire permutation matrix P associated with the transmission bus, and wherein the set of original symbols represents a set of input bits, and a decoder configured to generate a set of output bits based on the set of permuted symbols using a set of comparators having input weights based on a P-amenable orthogonal matrix, the P-amenable orthogonal matrix based on an orthogonal generating matrix and the permutation matrix P, wherein the set of output bits corresponds to the set of input bits.

In accordance with that least one embodiment, the plurality of comparators are configured to generate a set of comparator outputs, and wherein the set of output bits corresponds to the set of comparator outputs.

In accordance with that least one embodiment, the plurality of comparators are configured to generate a set of comparator outputs, and generating the set of output bits comprises a logical reordering of the comparator outputs.

In accordance with that least one embodiment, the plurality of comparators are configured to generate a set of comparator outputs, and generating the set of output bits comprises a binary inversion of at least one of the comparator outputs.

In accordance with that least one embodiment, the permutation matrix P is represented as:

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$$P = \begin{pmatrix} 1 & 0 & \dots & 0 & 0 \\ 0 & 1 & \dots & 0 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & \dots & 1 & 0 \\ 0 & 0 & \dots & 0 & 1 \end{pmatrix}.$$

In accordance with that least one embodiment, the permutation matrix P corresponds to a full reversal matrix R, the full reversal matrix R represented as:

$$R = \begin{pmatrix} 0 & 0 & \dots & 0 & 1 \\ 0 & 0 & \dots & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 1 & \dots & 0 & 0 \\ 1 & 0 & \dots & 0 & 0 \end{pmatrix}$$

In accordance with that least one embodiment, the orthogonal generating matrix is represented by M:

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -4 \end{pmatrix},$$

the P-amenable orthogonal matrix is represented by M':

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & -1 & 0 & -1 & 1 \\ 1 & 1 & -4 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4]$ and a set of comparator outputs represented as $[-x_1 \ -x_2 \ x_3 \ x_4]$, forming the set of output bits comprises inverting comparator outputs $-x_1$ and $-x_2$.

In accordance with that least one embodiment, the orthogonal generating matrix is represented by M:

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1 & 1 & -1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 1 & -2 & -2 \end{pmatrix},$$

the P-amenable orthogonal matrix is represented by M':

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 1 & -1 & 0 & 0 & -1 & 1 \\ 1 & 1 & -2 & -2 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4 \ x_5]$ and a set of comparator outputs represented as $[-x_1 -x_2 -x_3 \ x_4 \ x_5]$, forming the set of output bits comprises inverting comparator outputs $-x_1$, $-x_2$, and $-x_3$.

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In accordance with that least one embodiment, an apparatus comprises an encoder configured to receive a set of input bits and responsively generate a set of symbols of a codeword based on the set of input bits and a P-amenable orthogonal matrix, the P-amenable orthogonal matrix based on orthogonal generating matrix and a permutation matrix P, and a transmission bus configured to form a set of permuted symbols, wherein the permuted symbols represent a wire permutation of the set of symbols of the codeword, the wire permutation based on the permutation matrix P, the permutation matrix P associated with the transmission bus, and to transmit the set of permuted symbols.

In accordance with at least one embodiment, the P-amenable orthogonal matrix represents a permutation of columns of the orthogonal generating matrix.

We claim:

1. A method comprising:

receiving a set of permuted symbols on a transmission bus having a wire permutation, wherein the received set of permuted symbols correspond to an original set of symbols of a codeword permuted according to the wire permutation, the wire permutation representable by a permutation matrix P, the original set of symbols representing a set of input bits;

forming a set of output bits from the received set of permuted symbols using a set of comparators having input weights based on respective rows of a P-amenable orthogonal matrix, wherein the P-amenable orthogonal matrix is based on an orthogonal generating matrix and the permutation matrix P, the set of output bits corresponding to the set of input bits; and, outputting the set of output bits.

2. The method of claim 1, wherein forming the set of output bits further comprises generating a set of comparator outputs, wherein the comparator outputs correspond to the output bits.

3. The method of claim 1, wherein forming the set of output bits further comprises generating a set of comparator outputs, and performing a logical reordering of the set of comparator outputs.

4. The method of claim 1, wherein forming the set of output bits further comprises generating a set of comparator outputs, and performing a binary inversion of at least one of the comparator outputs.

5. The method of claim 1, wherein the P-amenable orthogonal matrix is representable as:

$$M' = \begin{pmatrix} 1 & 1 & 1 \\ 1 & 0 & -1 \\ 1 & -2 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2]$, a set of comparator outputs represented as $[-x_1 \ x_2]$, forming the set of output bits comprises a binary inversion of comparator output $-x_1$.

6. The method of claim 1, wherein the P-amenable orthogonal matrix is representable as:

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & -1 & 0 & -1 & 1 \\ 1 & 1 & -4 & 1 & 1 \end{pmatrix},$$

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and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4]$ a set of comparator outputs represented as $[-x_1 \ -x_2 \ x_3 \ x_4]$, forming the set of output bits comprises a binary inversion of comparator outputs $-x_1$ and $-x_2$.

7. The method of claim 1, wherein the P-amenable orthogonal matrix is representable as:

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 1 & -1 & 0 & 0 & -1 & 1 \\ 1 & 1 & -2 & -2 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4 \ x_5]$, a set of comparator outputs represented as $[-x_1 \ -x_2 \ -x_3 \ x_4 \ x_5]$, forming the set of output bits comprises a binary inversion of comparator outputs $-x_1$, $-x_2$, and $-x_3$.

8. The method of claim 1, wherein the codeword is part of an Orthogonal Differential Vector Signaling (ODVS) code.

9. The method of claim 1, wherein the permutation matrix P is a monomial matrix having a single '1' value in each column and in each row and '0' values elsewhere, each respective column associated with a respective symbol of the permuted set of symbols, wherein each respective column selects a respective symbol of the original set of symbols as the respective symbol of the permuted set of symbols, the selection based on a location of the '1' value in the respective column.

10. The method of claim 9, wherein the permutation matrix P is represented as:

$$P = \begin{pmatrix} 0 & 0 & \dots & 0 & 1 \\ 0 & 0 & \dots & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 1 & \dots & 0 & 0 \\ 1 & 0 & \dots & 0 & 0 \end{pmatrix},$$

corresponding to a full transmission bus reversal.

11. An apparatus comprising:

a transmission bus configured to receive a set of permuted symbols, wherein the set of permuted symbols represents a wire permutation of a set of original symbols based on a permutation matrix P, the permutation matrix P associated with the transmission bus, and wherein the set of original symbols represents a set of input bits; and,

a decoder configured to generate a set of output bits based on the set of permuted symbols using a set of comparators having input weights based on a P-amenable orthogonal matrix, the P-amenable orthogonal matrix based on an orthogonal generating matrix and the permutation matrix P, wherein the set of output bits corresponds to the set of input bits.

12. The apparatus of claim 11, wherein the set of comparators are configured to generate a set of comparator outputs, and wherein the set of output bits corresponds to the set of comparator outputs.

13. The apparatus of claim 11, wherein the set of comparators are configured to generate a set of comparator

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outputs, and generating the set of output bits comprises a logical reordering of the comparator outputs.

14. The apparatus of claim 11, wherein the set of comparators are configured to generate a set of comparator outputs, and generating the set of output bits comprises a binary inversion of at least one of the comparator outputs.

15. The apparatus of claim 11, wherein the orthogonal generating matrix is represented by M:

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 1 & 1 & -1 & -1 & 0 \\ 1 & 1 & 1 & 1 & -4 \end{pmatrix},$$

the P-amenable orthogonal matrix is represented by M':

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & -1 & 0 \\ 1 & -1 & 0 & -1 & 1 \\ 1 & 1 & -4 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4]$ and a set of comparator outputs represented as $[-x_1 \ -x_2 \ x_3 \ x_4]$, forming the set of output bits comprises inverting comparator outputs $-x_1$ and $-x_2$.

16. The apparatus of claim 11, wherein the orthogonal generating matrix is represented by M:

$$M = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 \\ 1 & 1 & -1 & -1 & 0 & 0 \\ 1 & 1 & 1 & 1 & -2 & -2 \end{pmatrix},$$

the P-amenable orthogonal matrix is represented by M':

$$M' = \begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 & 0 & -1 \\ 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 \\ 1 & -1 & 0 & 0 & -1 & 1 \\ 1 & 1 & -2 & -2 & 1 & 1 \end{pmatrix},$$

and for a set of input bits represented as $[x_1 \ x_2 \ x_3 \ x_4 \ x_5]$ and a set of comparator outputs represented as $[-x_1 \ -x_2 \ -x_3 \ x_4 \ x_5]$, forming the set of output bits comprises inverting comparator outputs $-x_1$, $-x_2$, and $-x_3$.

17. The apparatus of claim 11, wherein the permutation matrix P is a monomial matrix having a single '1' value in each column and in each row and '0' values elsewhere, each respective column associated with a respective symbol of the permuted set of symbols, wherein each respective column selects a respective symbol of the original set of symbols as the respective symbol of the permuted set of symbols, the selection based on a location of the '1' value in the respective column.

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18. The apparatus of claim 17, wherein the permutation matrix P is represented as:

$$P = \begin{pmatrix} 0 & 0 & \dots & 0 & 1 \\ 0 & 0 & \dots & 1 & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 1 & \dots & 0 & 0 \\ 1 & 0 & \dots & 0 & 0 \end{pmatrix},$$

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corresponding to a full transmission bus reversal.

19. An apparatus comprising:

an encoder configured to receive a set of input bits and
responsively generate a set of symbols of a codeword 15
based on the set of input bits and a P-amenable orthogo-
nal matrix, the P-amenable orthogonal matrix based on
orthogonal generating matrix and a permutation matrix
P; and,

a transmission bus configured to form a set of permuted 20
symbols, wherein the set of permuted symbols repre-
sents a wire permutation of the set of symbols of the
codeword, the wire permutation based on the permu-
tation matrix P, the permutation matrix P associated
with the transmission bus, and to transmit the set of 25
permuted symbols.

20. The apparatus of claim 19, wherein the P-amenable
orthogonal matrix represents a permutation of columns of
the orthogonal generating matrix.

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